CLAIMS

I CLAIM:

1. A method of making toroidal magnetic memory cells comprising:

providing at least one first conductor;

depositing a hard layer of material upon the first conductor;

forming from the hard layer at least one pillar;

depositing a ferromagnetic material about the pillar;

forming an annular data layer from the ferromagnetic material about the pillar;

depositing a junction stack upon at least a portion of the data layer;

depositing a dielectric upon the junction stack; and

planarizing the dielectric to expose the at least one pillar.

2. The method of claim 1, wherein the formation of the at least one pillar further includes:

depositing a photoresist upon the material layer;

masking the photoresist to provide at least two areas of photoresist protected material, the first an annular ring concentric about a second area, the photoresist being developed to remove the photoresist from the non-protected area, thereby exposing at least one portion of the material layer; and

ion etching about the remaining photoresist to substantially remove at least a portion of the exposed portion of the material layer, the second protected area defining the pillar, the first protected area defining a substantially annular wall concentric about the pillar.

3. The method of claim 2, wherein the ion etching is accomplished by RIE.

4. The method of claim 1, wherein the planarizing is by chemical mechanical polishing (CMP).

5. The method of claim 1, wherein the material of the hard layer is selected from the group consisting of Silicon, Silicon Dioxide, Silicon Carbon, and Silicon Nitride.

6. The method of claim 1, wherein the at least one pillar is cylindrical.

7. The method of claim 1, wherein the junction stack is asymmetrically placed upon the data layer.

8. The method of claim 1, wherein the resulting toroidal memory cell has a diameter of about 50 nanometers to 150 nanometers.

9. The method of claim 1, wherein the at least one pillar is characterized by a length, a width and a height, the aspect ratio of the height to the length to the width being substantially between 2 and 30.

10. The method of claim 1, wherein the material of the hard layer is conductive material.

11. The method of claim 10, wherein the at lest one pillar forms a second conductor through the annular data layer.

12. The method of claim 1, further including forming a third conductor in electrical contact with the junction stack.

13. The method of claim 1, wherein the junction stack is characterized by an intermediate layer in contact with the data layer, and a reference layer in contact with the intermediate layer, opposite from the data layer.

14. The method of claim 13, wherein the reference layer is a soft-reference layer.

15. The method of claim 1, further including replacing the at least one pillar with a conductive material after planarizing.

16. The method of claim 1, further comprising at least two first conductors, wherein the junction stack is deposited upon one of the first at least two first conductors before the data layer is deposited.

17. A method of making toroidal magnetic memory cells comprising:

providing a wafer substrate;

providing at least one first conductor upon the wafer substrate;

depositing a hard layer of material upon the first conductor;

forming from the hard layer at least one pillar;

forming from the hard layer at least one substantially annular wall about each pillar, the annular wall about the pillar defining a substantially annular slot;

depositing a ferromagnetic data layer within the annular slot;

depositing a junction stack upon at least a portion of the data layer;

depositing a dielectric upon the junction stack to insulate the junction stack; and

planarizing the dielectric to expose the at least one pillar.

18. The method of claim 17, wherein the formation of the at least one pillar and the annular wall further includes:

depositing a photoresist upon the material layer;

masking the photoresist to provide at least two areas of photoresist protected material, the first an annular ring concentric about a second area, the photoresist being developed to remove the photoresist from the non-protected area, thereby exposing at least one portion of the material layer; and

ion etching about the remaining photoresist to substantially remove at least a portion of the exposed portion of the material layer, the second protected area defining the pillar, the first protected area defining a substantially annular wall concentric about the pillar.

19. The method of claim 18, wherein the ion etching is accomplished by RIE.

20. The method of claim 17, wherein the planarizing is by chemical mechanical polishing (CMP).

21. The method of claim 17, wherein the material of the hard layer is selected from the group consisting of Silicon, Silicon Dioxide, Silicon Carbon, and Silicon Nitride.

22. The method of claim 17, wherein the at least one pillar is cylindrical.

23. The method of claim 17, wherein the junction stack is asymmetrically placed upon the data layer.

24. The method of claim 17, wherein the resulting toroidal memory cell has a diameter of about 50 nanometers to 150 nanometers.

25. The method of claim 17, wherein the at least one pillar is characterized by a length, a width and a height, the aspect ratio of the height to the length to the width being substantially between 2 and 30.

26. The method of claim 17, wherein the material of the hard layer is conductive material.

27. The method of claim 26, wherein the at least one pillar forms a second conductor through the ferromagnetic data layer.

28. The method of claim 17, further including forming a third conductor in electrical contact with the junction stack.

29. The method of claim 17, wherein the junction stack is characterized by an intermediate layer in contact with the data layer, and a reference layer in contact with the intermediate layer, opposite from the data layer.

30. The method of claim 29, wherein the reference layer is a soft-reference layer.

31. The method of claim 17, further including removing the annular wall after the ferromagnetic data layer is deposited.

32. The method of claim 17, further including replacing the at least one pillar with a conductive material after planarizing.

33. The method of claim 17, further comprising at least two first conductors, wherein the junction stack is deposited upon one of the first at least two first conductors before the data layer is deposited.

34. A method of making toroidal magnetic memory cells having a common conductor, a read conductor and a write conductor, comprising:

depositing at least one common conductive layer upon a wafer substrate;

depositing a hard layer of material upon the common conductor layer;

depositing a photoresist upon the material layer to provide at least two areas of photoresist protected material, the first an annular ring concentric about a second protected area, the photoresist being developed to remove the photoresist from the non-protected area, thereby exposing at least one portion of the material layer;

ion etching about the remaining photoresist to substantially remove at least a portion of the exposed portion of the material layer, the second protected area defining a pillar, the first protected area defining a substantially annular wall concentric about the pillar, the wall further defining a substantially annular slot about the pillar;

depositing a ferromagnetic data layer within the annular slot;

depositing a junction stack upon at least a portion of the data layer;

removing the annular wall from around the data layer;

depositing a dielectric upon the junction stack to insulate the junction stack;

planarizing the dielectric to expose the at least one pillar;

depositing a read conductor in electrical contact with the junction stack;

wherein the pillar occupies the position of the write conductor, passing through the data layer and in electrical contact with the common conductive layer.

35. The method of claim 34, wherein the at least one pillar is conductive and acts as the write conductor.

36. The method of claim 34, wherein the ion etching is accomplished by RIE.

37. The method of claim 34, wherein the planarizing is by chemical mechanical polishing (CMP).

38. The method of claim 34, wherein the material of the hard layer is selected from the group consisting of Silicon, Silicon Dioxide, Silicon Carbon, and Silicon Nitride.

39. The method of claim 34, wherein the at least one pillar is cylindrical.

40. The method of claim 34, wherein the junction stack is asymmetrically placed upon the data layer.

41. The method of claim 34, wherein the resulting toroidal memory cell has a diameter of about 50 nanometers to 150 nanometers.

42. The method of claim 34, wherein the junction stack is characterized by an intermediate layer in contact with the data layer, and a reference layer in contact with the intermediate layer, opposite from the data layer.

43. The method of claim 42, wherein the reference layer is a soft-reference layer.

44. The method of claim 34, further including replacing the at least one pillar with a conductive material after planarizing.

45. The method of claim 34, further comprising at least two first conductors, wherein the junction stack is deposited upon one of the first at least two first conductors before the data layer is deposited.